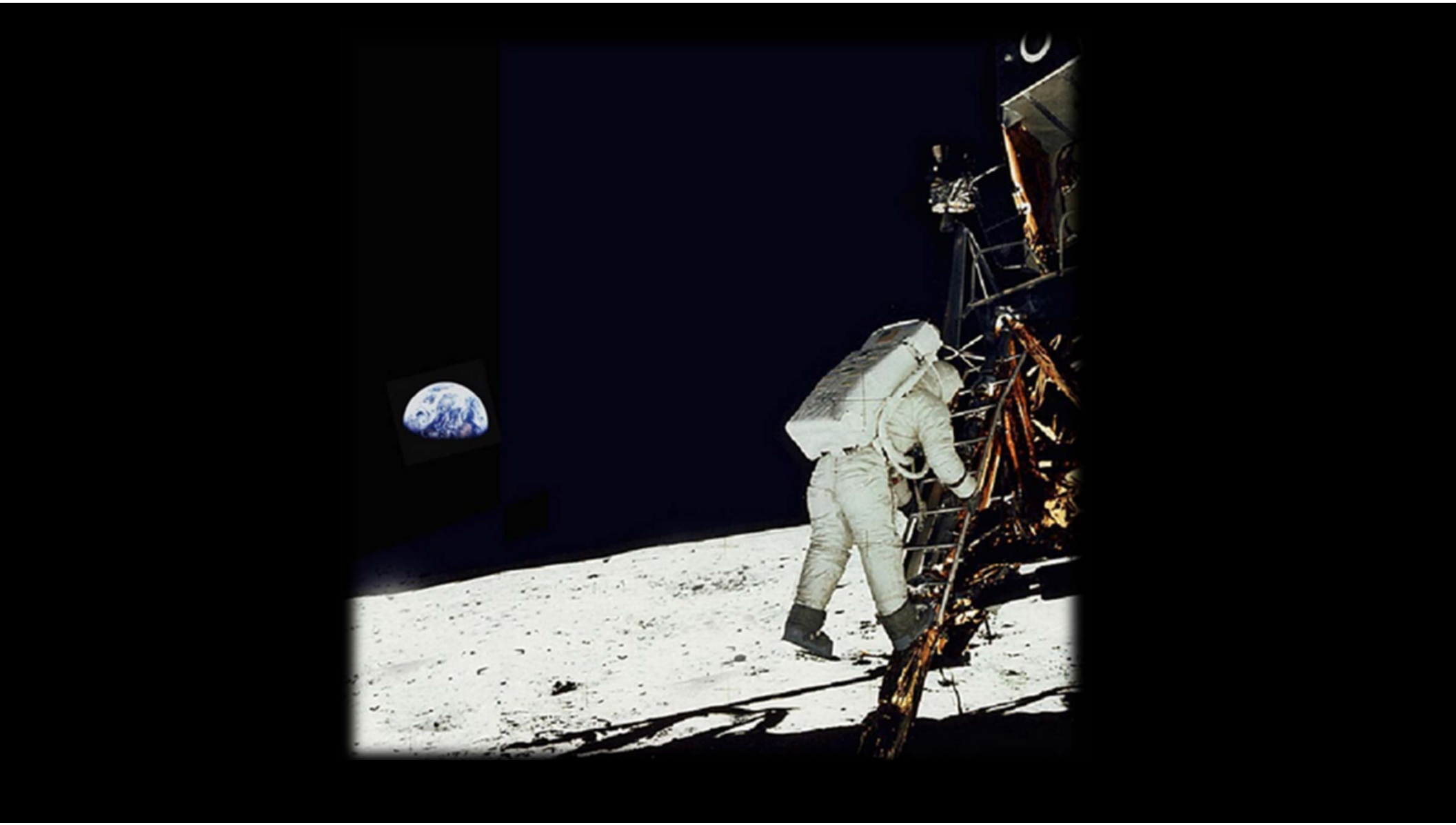
SAN LORENZO VALLEY AMATEUR RADIO CLUB

NASA Computer Memory and More

The 50th anniversary of the Apollo 11 moon landing is approaching! July 20, 1969

While at IBM Federal Systems Division located in Owego, NY Lynn Liebschutz worked on the On Board Computer memory system for Gemini and follow-on guidance and navigation. A similar memory system in a much more robust computer existed in the Instrument Unit ring stacked in NASA's three-stage Saturn V launch vehicle. We'll be hearing about this highly reliable computing system, and Lynn ~~probably~~ will mention earlier and later projects, such as a wirelessly communicating computer system for the National Bureau of Standards, radiation hardened computer memory systems, and even bubble memory.



Lynn Liebschutz, Technologist / Western Digital Corporation

lynn.liebschutz@wdc.com

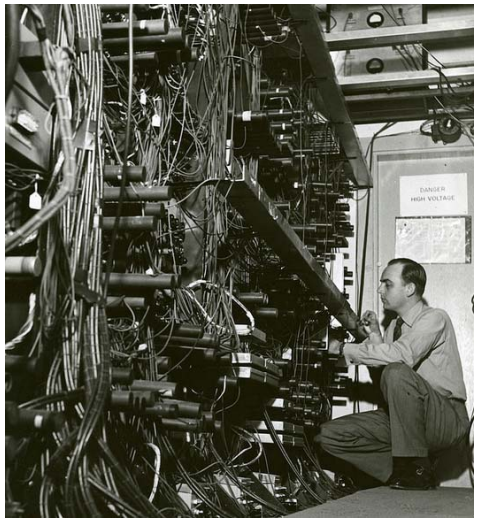
- **BS Physics, Carnegie Institute of Technology / now Carnegie Mellon University**
- **MS Physics Program, SUNY Binghamton, Syracuse University**

- **NBS Data Processing Laboratory; Washington, DC**
- **Burroughs Corporation Development Lab; Paoli, PA**
- **IBM Federal Systems Division; Owego, NY**
- **IBM Office Products Division; Lexington, KY**
- **IBM Systems Development Division and General Products Division; San Jose, CA 1976**
  - ↳ **Hitachi GST**
    - ↳ **HGST**
      - ↳ **HGST / WD**
        - ↳ **WDC**

SEAC – Standards Eastern Automatic Computer

- **Almost 'Last' of the vacuum tube machines**

SEAC (***S**tandards **E**astern **A**utomatic **C**omputer* or ***S**tandards **E**lectronic **A**utomatic **C**omputer*)[2] was a first-generation electronic computer, **built in 1950** by the U.S. National Bureau of Standards (NBS) and was initially called the *National Bureau of Standards Interim Computer*, because it was a small-scale computer designed to be built quickly and put into operation while the NBS waited for more powerful computers to be completed (the DYSEAC). The team that developed SEAC was organized by Samuel N. Alexander. SEAC was demonstrated in April 1950 and was dedicated on June 1950; it is claimed to be the **first fully operational stored-program electronic computer in the US**.



https://en.wikipedia.org/wiki/SEAC_(computer)

SEAC Description

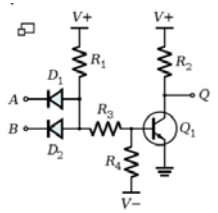
Based on EDVAC, SEAC used only 747 vacuum tubes (a small number for the time) eventually expanded to 1,500 tubes. It had 10,500 germanium diodes which performed all of the logic functions (see the article diode–transistor logic for the working principles of diode logic), later expanded to 16,000 diodes. It was the first computer to do most of its logic with solid-state devices. The tubes were used for amplification, inversion and storing information in dynamic flip-flops.[8] The machine used 64 acoustic delay lines to store 512 words of memory, with each word being 45 bits in size. The clock rate was kept low (1 MHz).

64 * 512 * 45 = 1.5 Mb

The computer's instruction set consisted of only 11 types of instructions: fixed-point addition, subtraction, multiplication, and division; comparison, and input & output. It eventually expanded to 16 instructions.

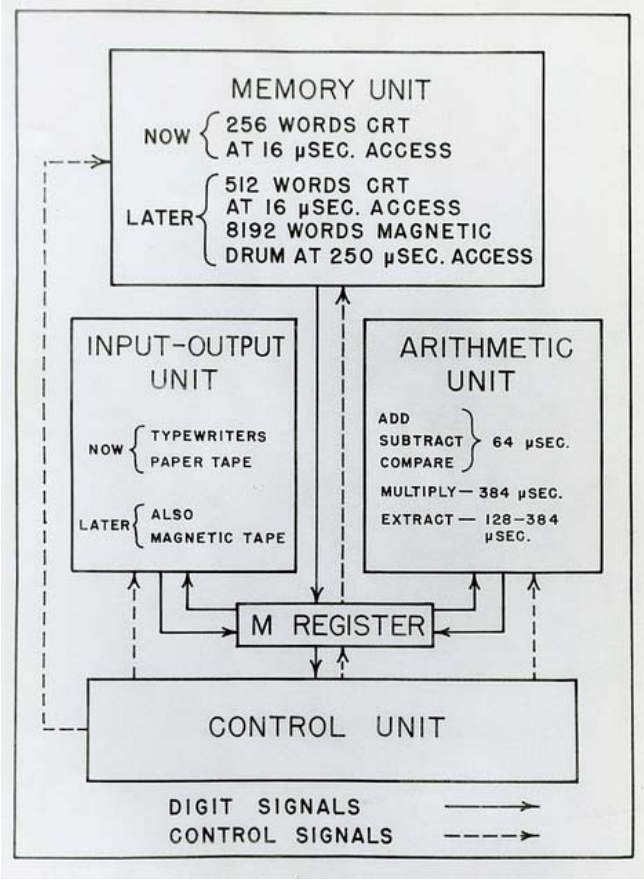
The addition time was 864 microseconds and the multiplication time was 2,980 microseconds (i.e. close to 3 milliseconds).

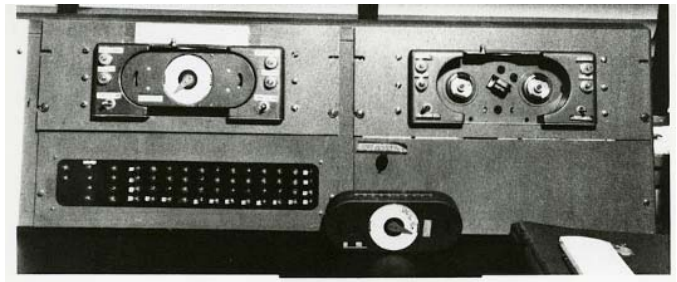
Weight: 3,000 pounds (1.5 short tons; 1.4 t) (Central Machine).[2]



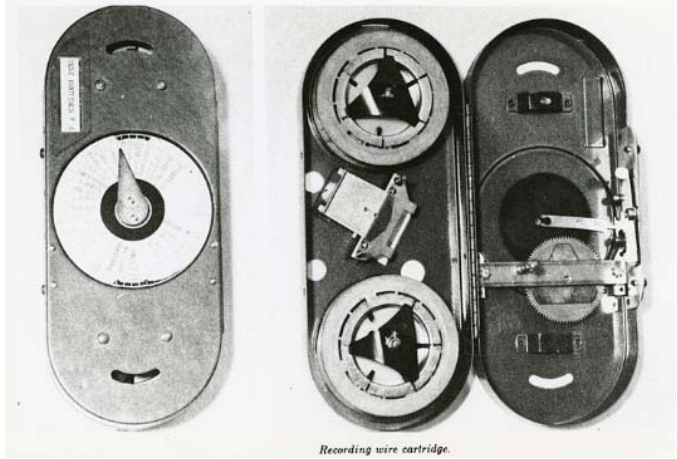
https://www.revolvy.com/page/SEAC-%28computer%29

SEAC Organization & Auxiliary Storage





SEAC input and output wire drives.

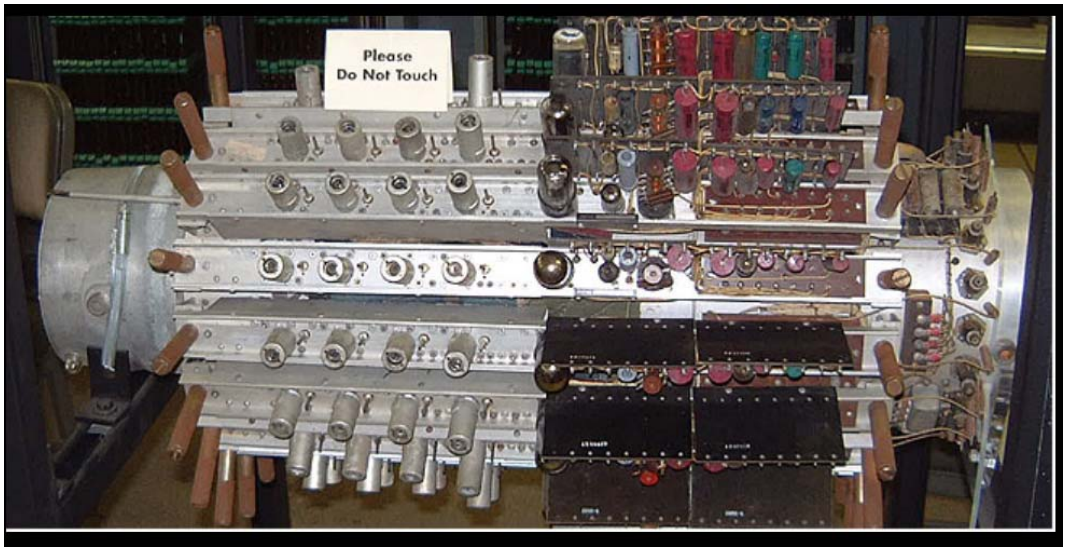


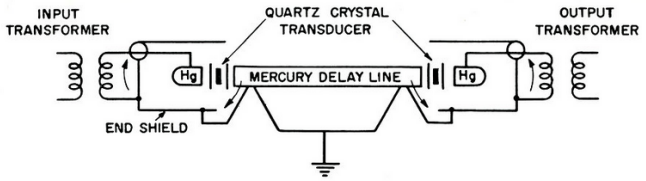
Recording wire cartridge.

- **Wire recording cartridge for auxiliary data.**
- **630 K b**
- **1800 ft wire at 8 ft/s – about 4 minutes.**

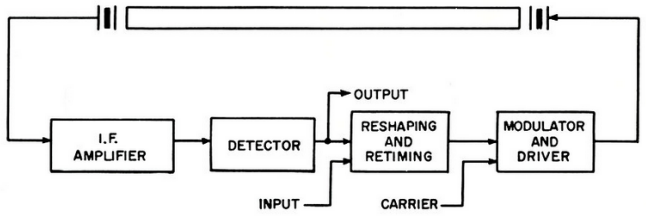
http://ed-thelen.org/comp-hist/SEAC&DYSEAC-6-150.pdf

Acoustic Mercury Memory





Schematic diagram of circuit connections to the acoustic delay line used in NBS mercury memory.



Block diagram of the mercury memory system.

64 Hg tubes 512 words 45 b / word = 1.5 Mb

Hg = 1450 m/s vs air 340 m/s vs metal 5800 m/s

256 * 35 = 9K bits

16 * 16 * 35 = 9K bits

https://en.wikipedia.org/wiki/Delay_line_memory#Mercury_delay_lines

Williams Tube Memory

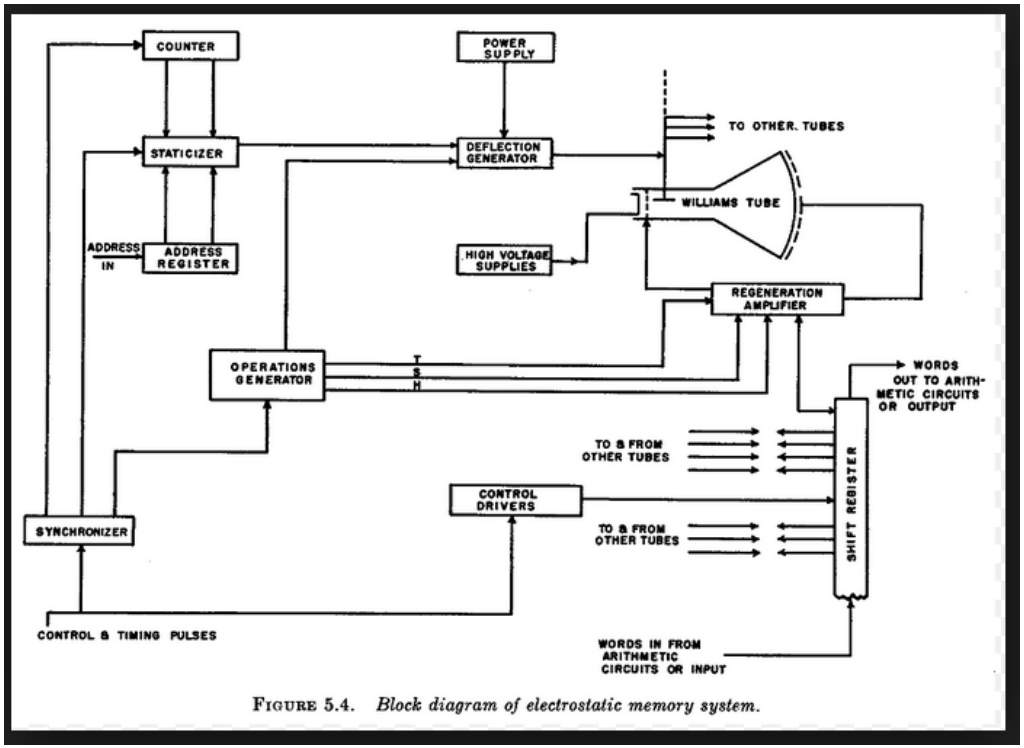
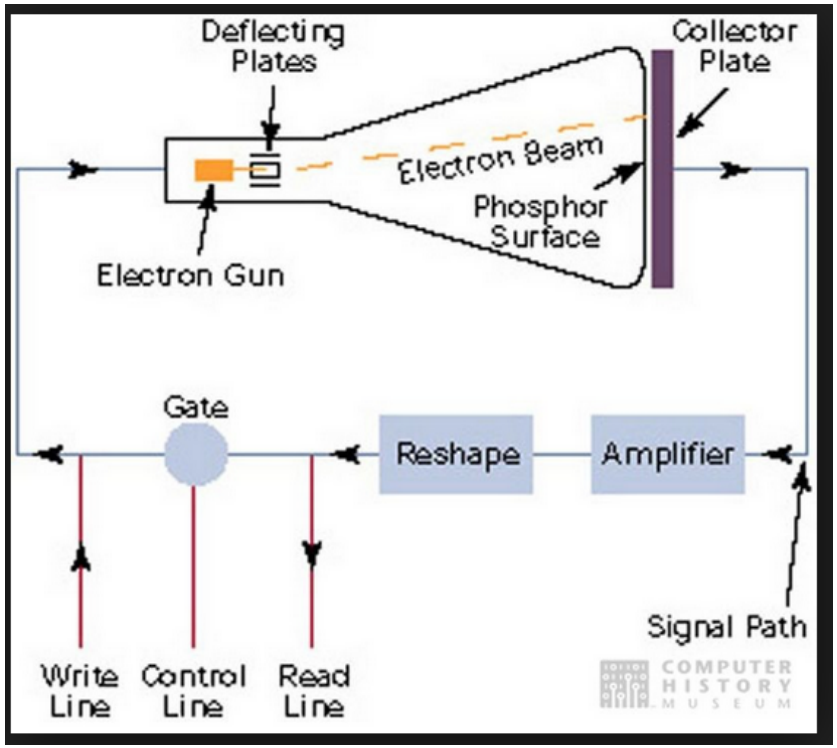


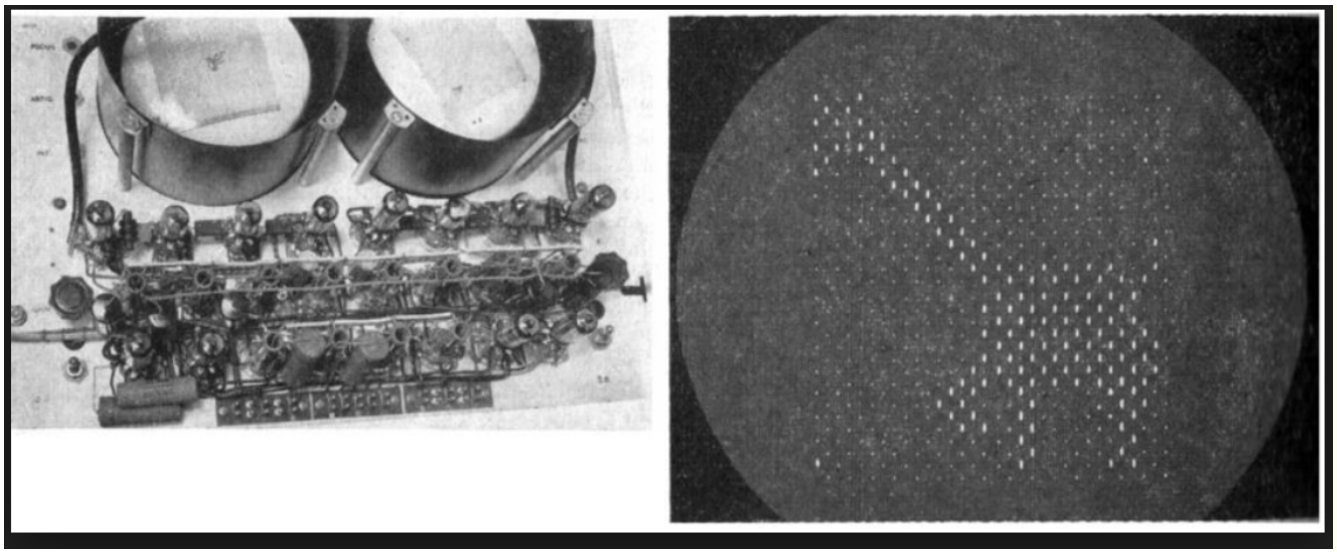
FIGURE 5.4. *Block diagram of electrostatic memory system.*

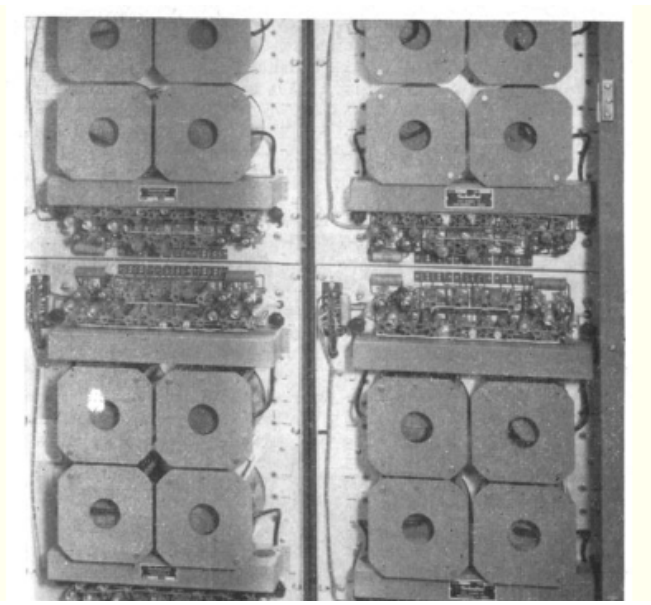


23 Kb / CRT @ 21 K b/s x 16 = 377 Kb
12 us / bit or 6,000 us / refresh

https://www.radiomuseum.org/forum/williams_kilburn_williams_kilburn_ram.html

Williams Tube Memory





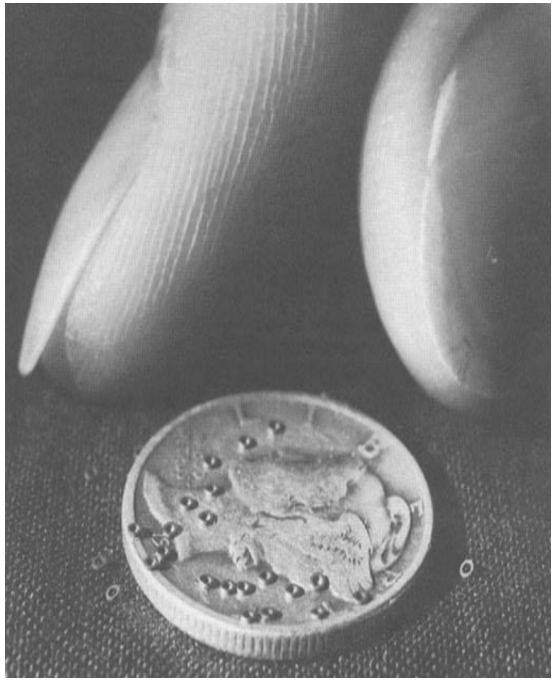
CRT & Electronics **CRT w 1's & 0's** **16 CRT Memory System**

https://www.radiomuseum.org/forum/williams_kilburn_williams_kilburn_ram.html

Core memory

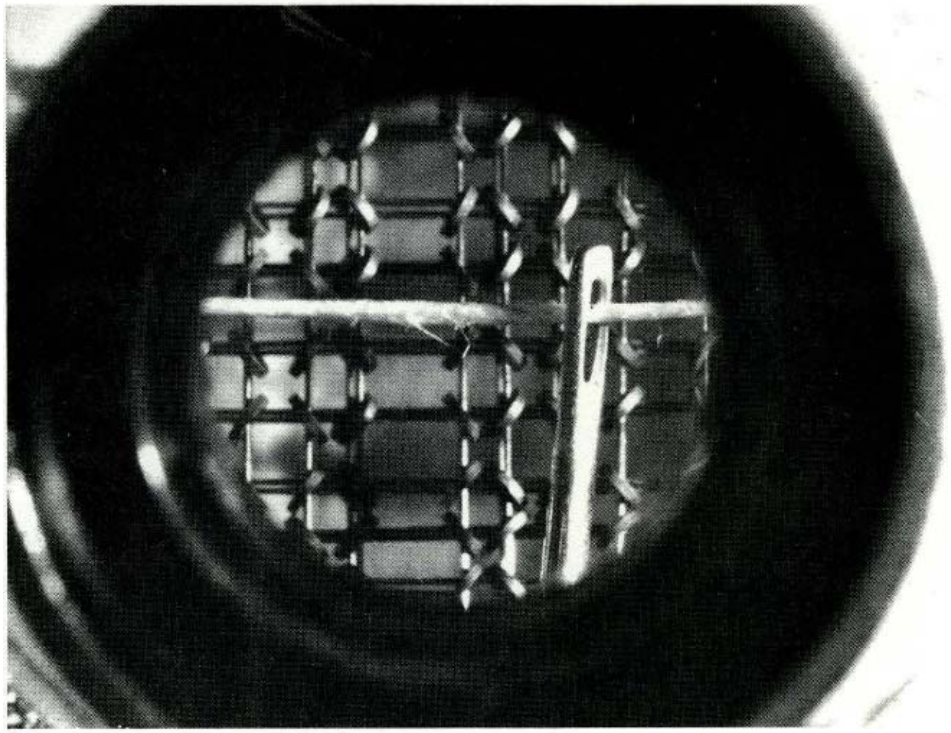
In System 4 Pi, the ROS microprogrammed control is implemented with magnetic cores 0.007 inner diameter and 0.012 outer diameter.
The cores are automatically wired into a word-organized array.

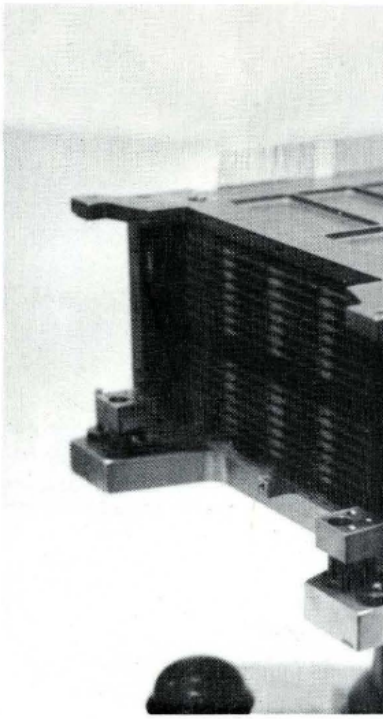
Figure 1-4. M



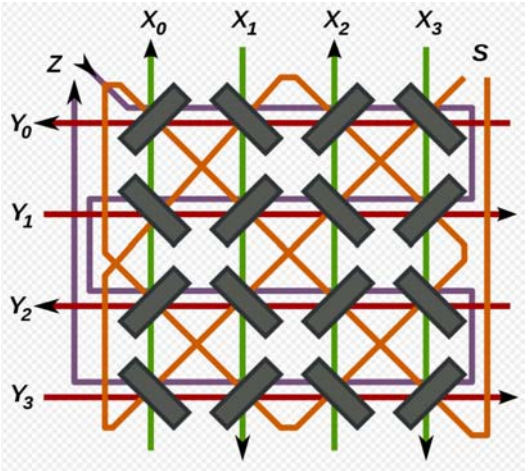
0.020 / 0.040 in

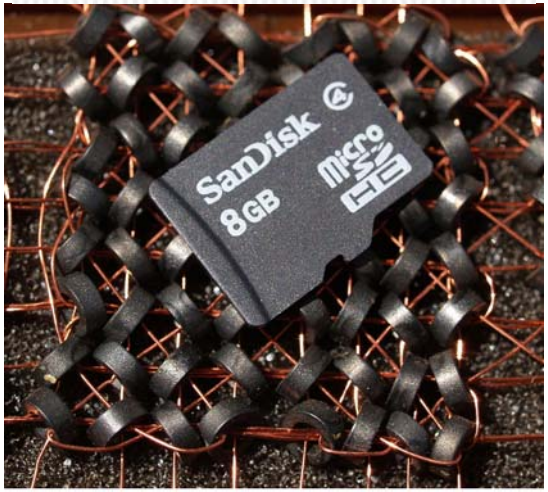
(0.5 / 1.0 mm)

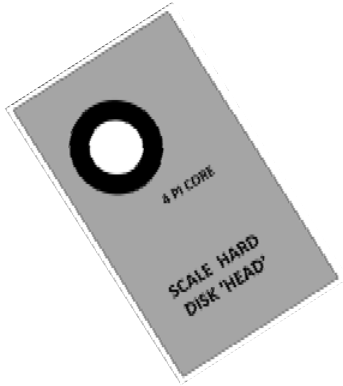




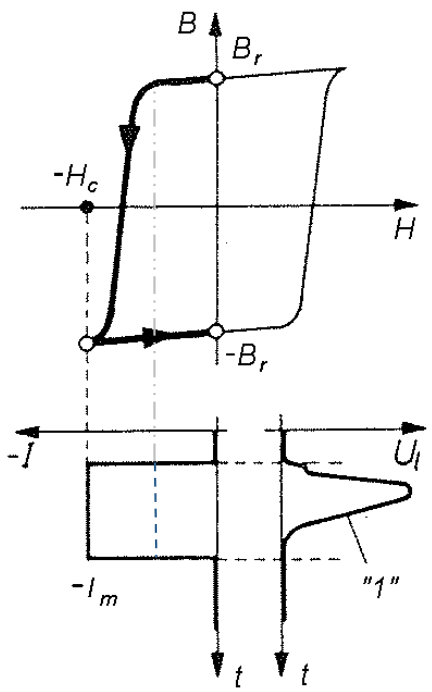
What & How



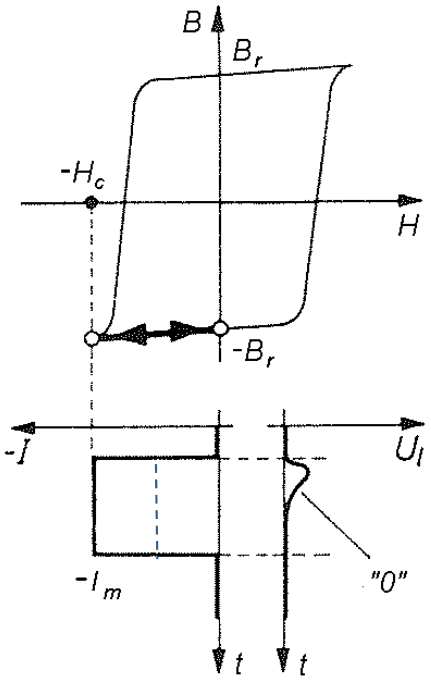




One

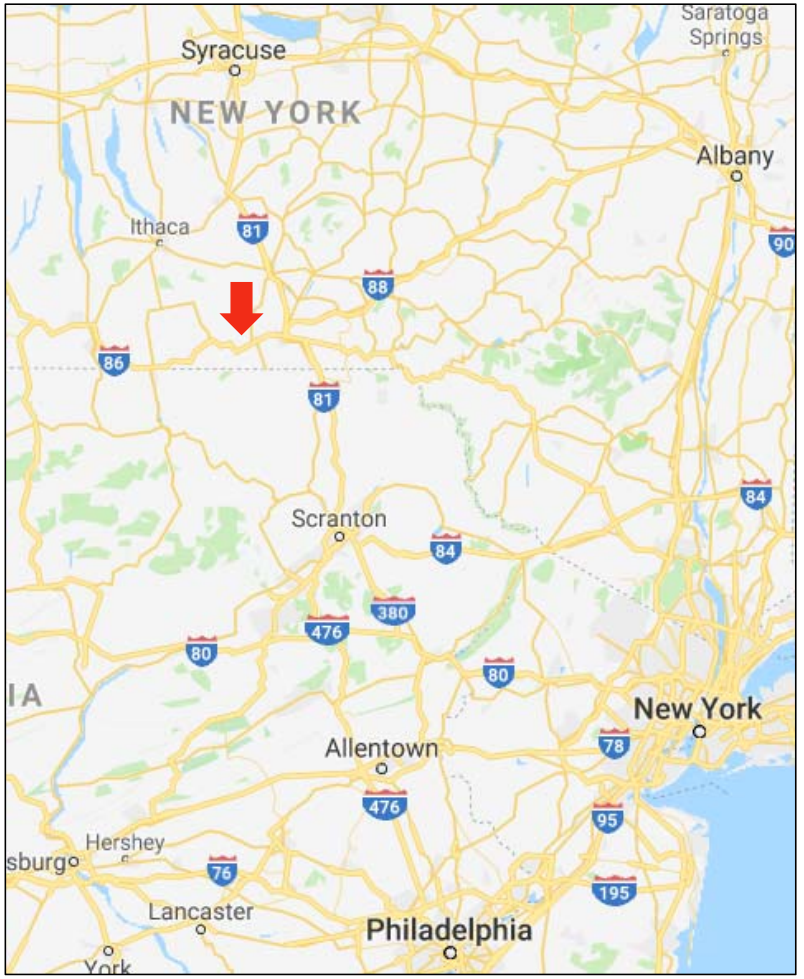


Zero



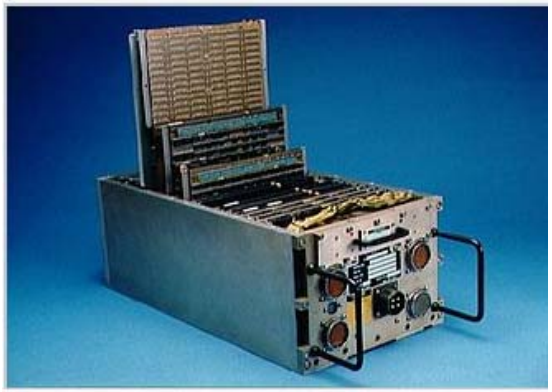
https://en.wikipedia.org/wiki/Magnetic-core_memory

IBM Federal Systems Division, Owego, NY now Lockheed-Martin

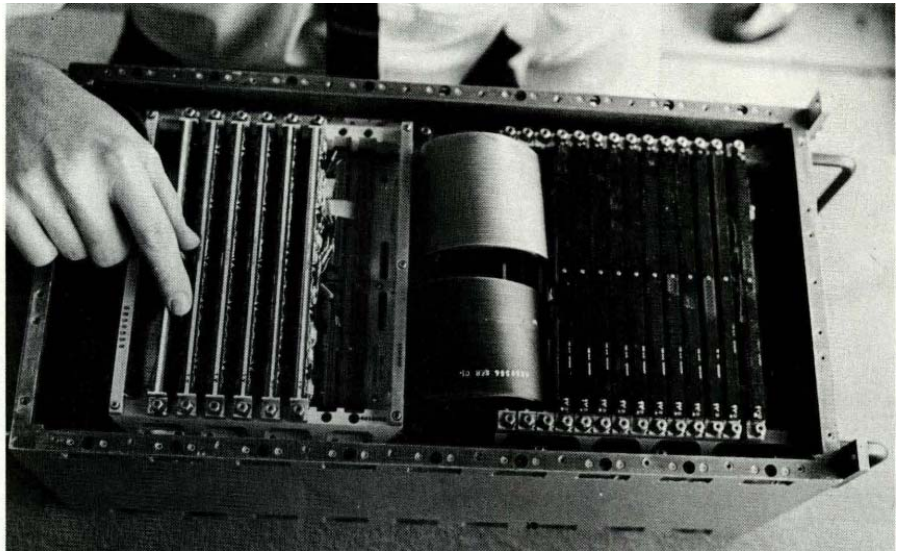


Standard AP Packaging is Rugged ATR ‘Box’

- **Main storage arrays of System/4 Pi were assembled from core planes that were militarized versions of those used in IBM System/360 computers**
- **Software was for both 360 and 4 Pi**
- **Model EP used an instruction subset of IBM System/360 (Model 44) - user programs could be checked on System/360**



The IBM AP-101S Space Shuttle General Purpose Computer is a member of the System/4 Pi family



IBM Gemini & Apollo ‘Computer’

The Gemini and Apollo computer systems were **custom-built processors**. Apollo did have an immediate predecessor, but the number of changes necessary before flight negated most of its resemblance to the Polaris system. To the contrary, Skylab and, later, the **Shuttle, used "off-the-shelf" IBM 4Pi series processors**, though they both needed the addition of a customized I/O system, a simpler and necessarily idiosyncratic component. By using existing computers, NASA avoided the serious problems associated with man-rating a new system encountered during the Apollo program.

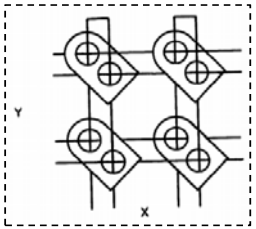
The **4Pi descended directly from the System 360 architecture** IBM developed in the early 1960s. Some 4Pis were at work in aircraft by the latter part of that decade. The top-of-the-line 4Pi is the AP-101, eventually used in the F-15, B-52, and Shuttle. The version on board Skylab was the TC-I, which used a 16-bit word, in contrast to the **AP-101's 32 bits**. A TC-I processor, an interface controller, an I/O assembly, and a power supply made up an ATMDC. **Each flight computer had a memory of 16,384 words**. This memory was a **destructive readout core memory**, which means that the bits were erased as they were read and that the memory location had to be refreshed with the contents of a buffer register, which saved a copy of the bits before they were passed on to the processor. The **memory was in two modules of 8K words each**. Addressing ranged from 0 to 8K, with a hardware switch determining which module was being accessed. The redundant computer system was composed of two processors attached to a single Workshop Computer Interface Unit. The unit consisted of two I/O sections (one for each computer), a common section, and a power supply. Only the I/O section connected to the active computer was powered. The inactive computer and its I/O section of the interface unit were not powered. The common section contained a 64-bit transfer register and timer associated with redundancy management[15].
The transfer register and timer were the only parts of Skylab that consisted of triple modular redundant (TMR) circuits[16]. Basically, TMR circuits sent signals in triplicate on separate channels and then voted. The single output from a **TMR voter** represented either two or three identical inputs.

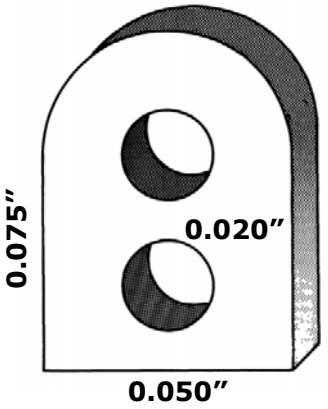
The Gemini Digital Computer was a transitional machine. Dale F. Bachman of IBM characterized it as the "last of a dying breed. It was an airborne computer, ruggedized, special purpose, and slow" . Nonetheless, its designers claim an impressive list of firsts :

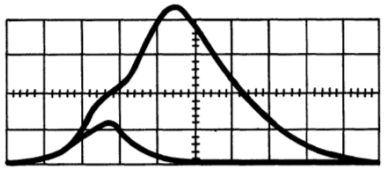
- **The first digital computer on a manned spacecraft.**
- **The first use of core memory with nondestructive readout. The machine was designed in an era of rotating drum memories, its designers considered it a step forward.**
- **IBM's first completely silicon semiconductor computer.**
- **The first to use glass delay lines as registers.**
- **Technologically advanced in the area of packaging density.**
- **The first airborne or space-borne computer to use an auxiliary memory.**

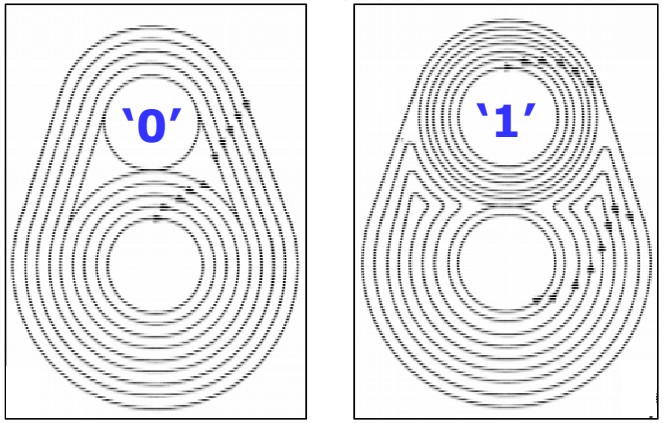
Non Destructive Core Memory

MARS -- Multi Aperture Reluctance Switch



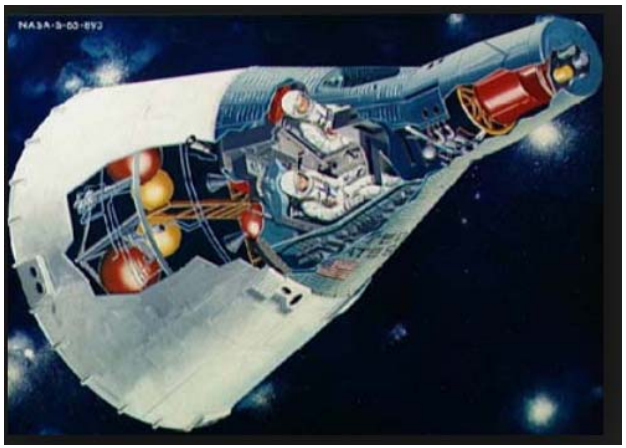


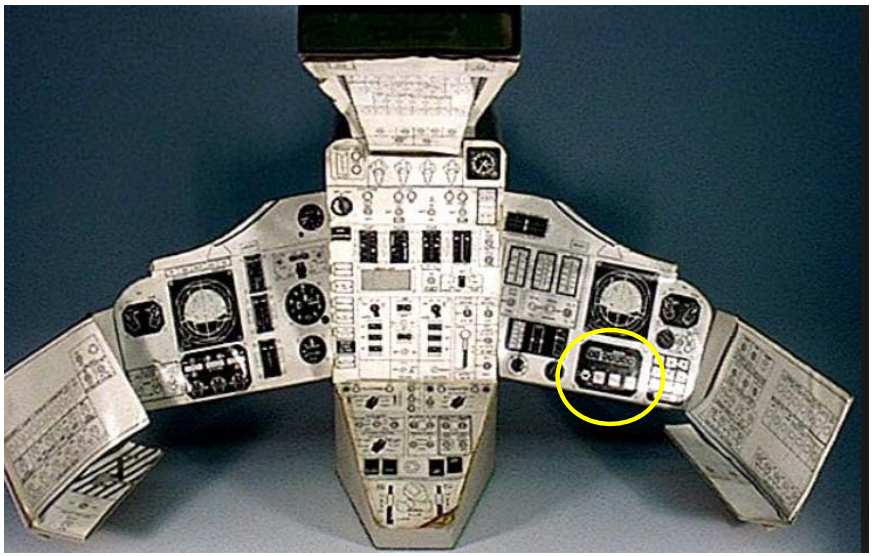




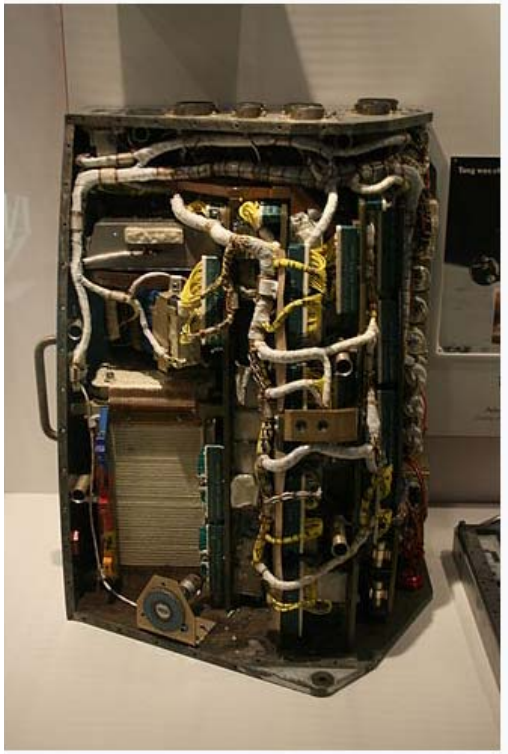
https://www.computer.org/csdl/proceedings/afips/1961/5058/00/50580443.pdf

Gemini Guidance Computer





Invented by	IBM Federal Systems Division
Manufacturer	IBM Federal Systems Division
Introduced	1965; 54 years ago
Discontinued	1966; 53 years ago
Type	Avionics Guidance Computer
Processor	Discrete IC RTL based
Frequency	7.143 kilohertz clock
Memory	39-bit words memory, each composed of three 13-bit syllables, 4096 words of memory, in a ferrite core array.
Ports	Modular Display Keyboard (MDK), Modular Display Readout (MDR), Attitude Control and Maneuver Electronics (ACME), Inertial Measurement Unit (IMU), Horizon Sensors, Time Reference System (TRS)[1]
Power consumption	28V DC
Weight	58.98 pounds (26.75 kg)
Dimensions	18.9"(H)×14.5"(W)×12.75"(D)

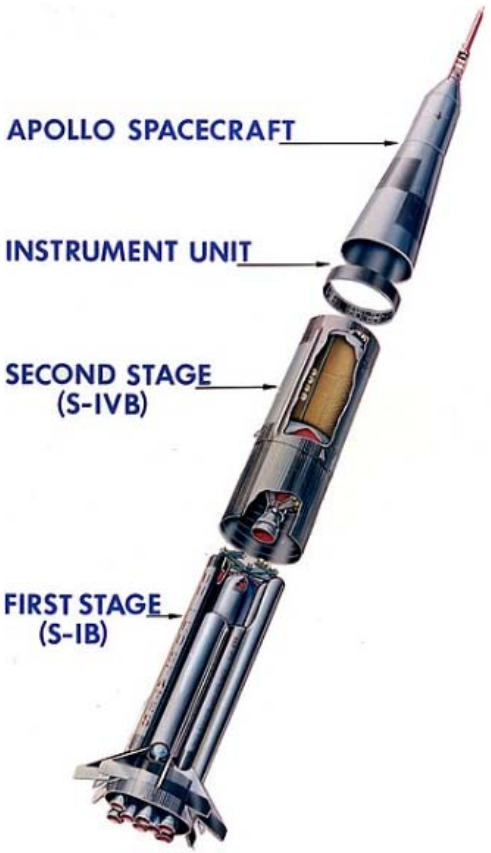


IBM 4 Pi AP Models

	Model TC	Model CP	Model EP
Applications	For satellites, tactical missiles, helicopters and other applications with overriding requirements for an exceptionally small, lightweight processor	For guidance and control, mobile battlefield systems, radar data correlation, weapons delivery, missile guidance and ELINT processing.	For military and space applications requiring extremely high-speed calculations involving large volumes of data, such as manned spacecraft and command and control systems.
Organization	general-purpose, parallel		
Main Storage	8,192 8-bit words, expandable to 65,536 words	8,192 32-bit words, expandable in 8,192 word increments	16,384 32-bit words, expandable in 8,192 word increments
Storage Cycle	2.5 μsec.		

Apollo

SATURN IB LAUNCH VEHICLE



CHARACTERISTICS

LENGTH (VEHICLE)	43 m
LENGTH (VEHICLE, SPACECRAFT, LES)	68 m
TOTAL DRY WEIGHT	50,000 Kg
TOTAL WET WEIGHT	568,200 Kg
WEIGHT AT LIFTOFF	588,000 Kg
EARTH ORBIT PAYLOAD	18,135 Kg

STAGES

FIRST (S-IB)

SIZE	6.5 x 24 m
ENGINES	8 H-1
THRUST (201 THRU 205)	724,800 Kg
(206 AND SUB)	742,920 Kg
PROPELLANT WEIGHT (LOX)	413,100 Kg
(RP-1)	127,300 Kg

SECOND (S-IVB)

SIZE	6.6 x 18.1 m
ENGINE	1 J-2
THRUST (201 THRU 207)	90,700/102,000 Kg
(208 AND SUB)	93,000/104,280 Kg
PROPELLANT WEIGHT (LOX)	86,000 Kg
(LH_2)	19,700 Kg

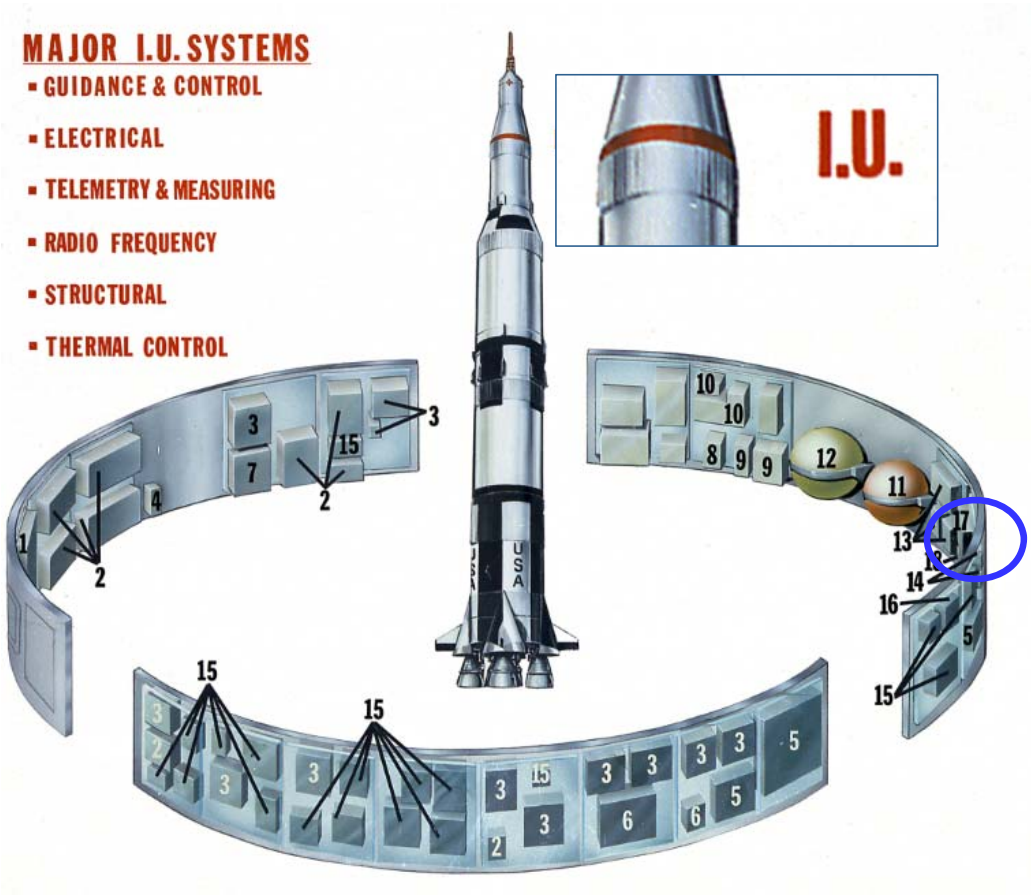
INSTRUMENT UNIT

SIZE	6.6 x .91 m
WEIGHT	2,038 Kg
GUIDANCE SYSTEM	INERTIAL

MSFC-71-PM 1100-29

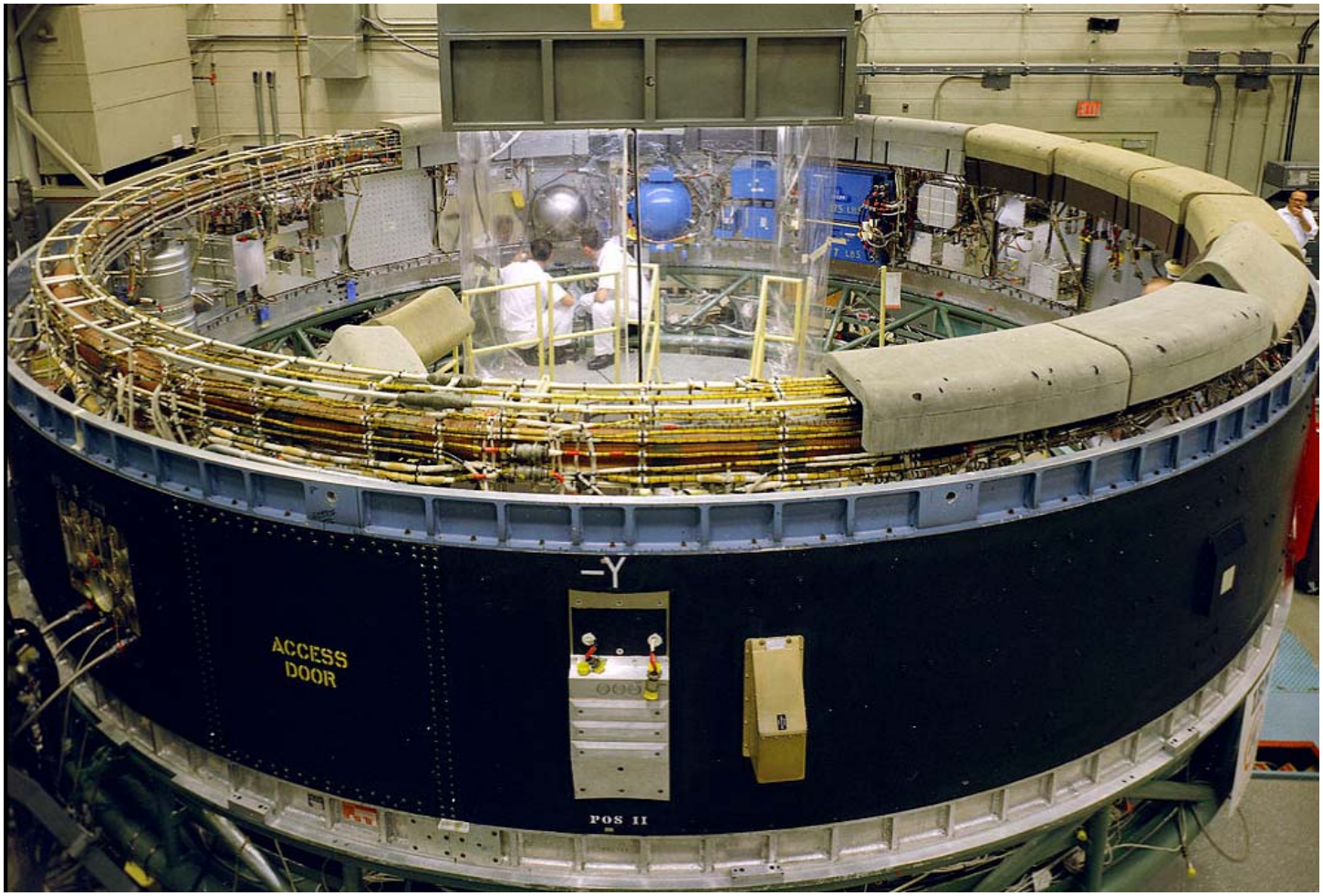
The Saturn V instrument unit, the "brains" of the Saturn V launch vehicle, was manufactured in the east high bay at International Business Machines (IBM) in Huntsville, Ala. IBM was the prime contractor for development and fabrication of the instrument unit. The instrument unit was designed by engineer's at NASA's Marshall Space Flight Center in Huntsville, and the ring configuration with electronics boxes mounted on the inside was based on the design of the instrument unit for the smaller Saturn I rocket. As with modern rocket avionics systems, the instrument unit was vital to the proper flight of the vehicle because it contained the navigation, guidance, control, and sequencing equipment. Three feet tall, twenty-one feet in diameter, and weighing about 4,000 pounds, the instrument unit was mounted atop the S-IVB, the rocket's third stage, between the S-IVB stage and the Apollo spacecraft.

SATURN 1B / V INSTRUMENT UNIT

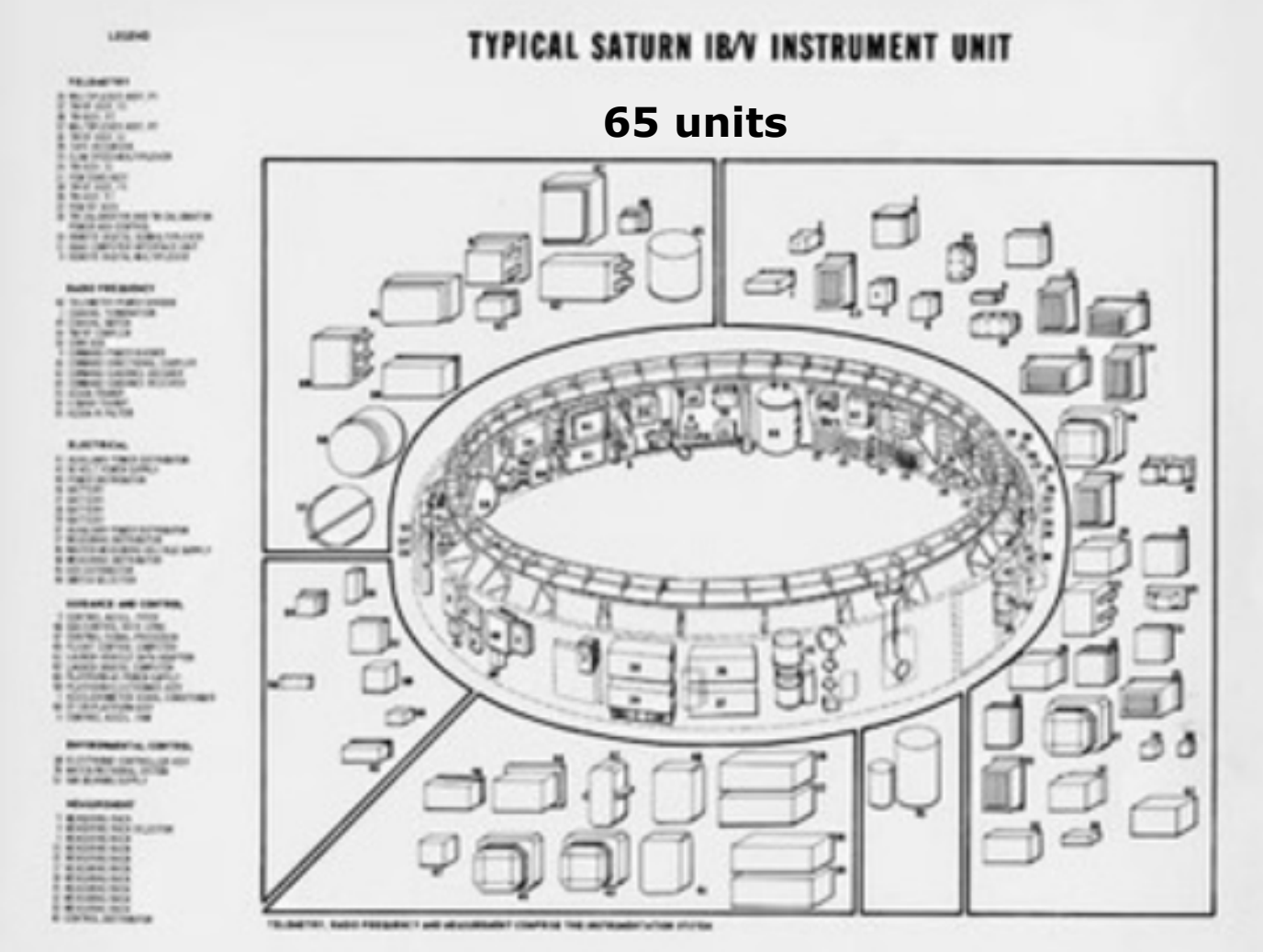


1. ENVIRONMENTAL CONTROL SYS.
2. ELECTRICAL POWER SYS.
3. MEASURING SYS.
4. CONTROL ACCELEROMETERS
5. CONTROL COMPUTER SYS.
6. EDS
7. RADAR ALTIMETER
8. C-BAND RADAR
9. AZUSA SYS.
10. MINITRACK SYS.
11. ST-124-M PLATFORM
12. PLATFORM AIR SUPPLY
13. PLATFORM ELECTRONICS
14. GUIDANCE COMMAND SYS.
15. TELEMETRY SYS.
16. SWITCH SELECTOR
17. GUIDANCE COMPUTER
18. DATA ADAPTER

IU - Φ 12.8 x 3 ft



Active Components



Sheet 14 / 19 with Launch Vehicle Guidance Computer

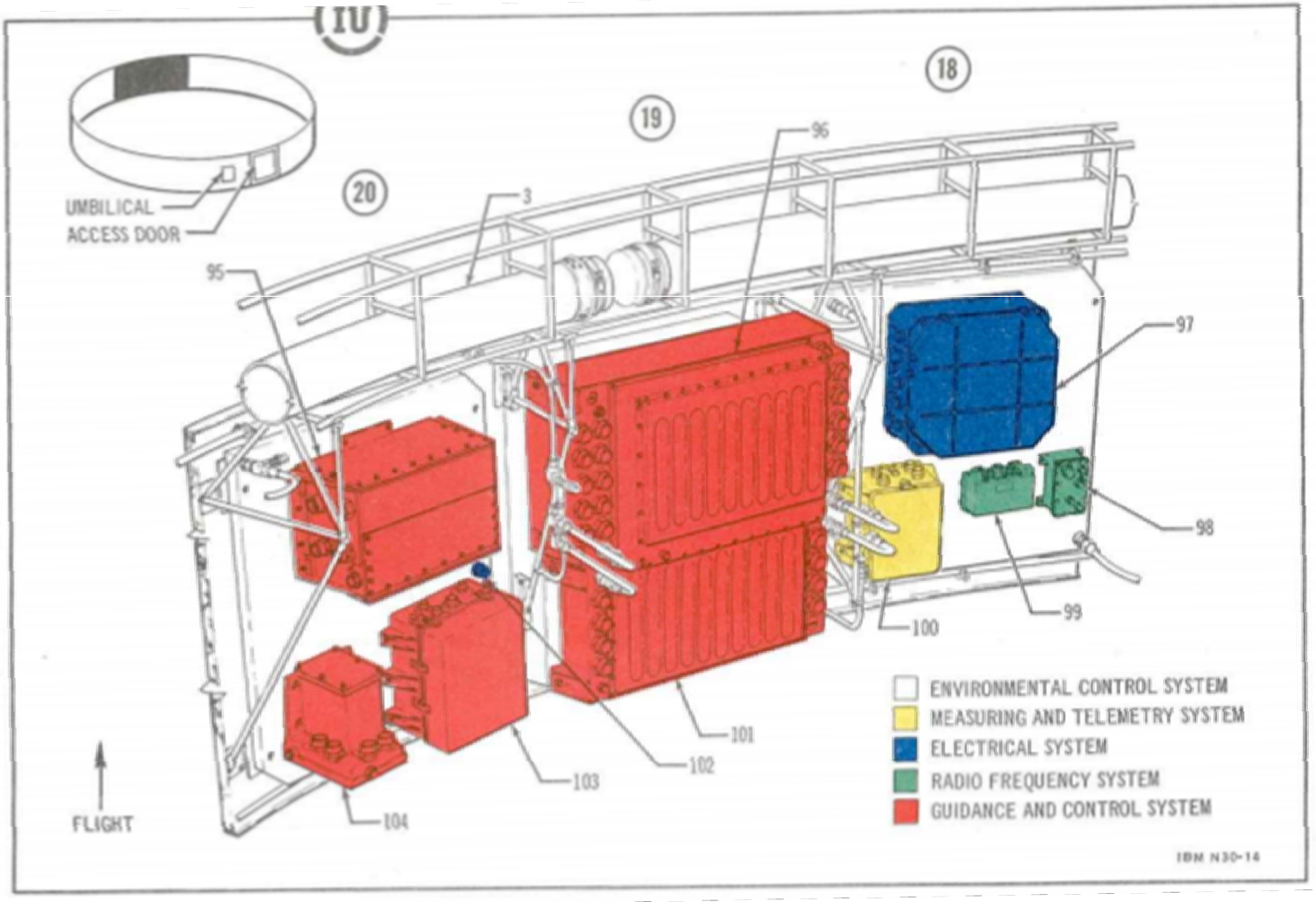


Figure 1. Instrument Unit Component Locations (sheet 14 of 19)

MSFC No. III-5-509-4

IBM No. 66-966-0006

DOCUMENT SCAN EXECUTED BY
MARK E. WELLS AND SCOTT B SCHNEEWEIS
29 FEBRUARY 2009

TECHNICAL MANUAL

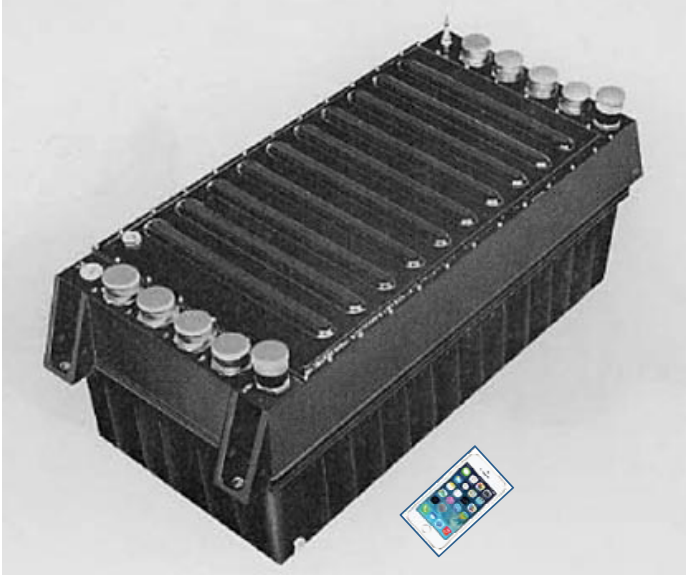
SATURN IB/V INSTRUMENT UNIT
SYSTEM DESCRIPTION
AND
COMPONENT DATA

(S-IU-201-212/501-515)

Prepared under Contract
NAS 8-14000
by
International Business Machines Corporation
Federal Systems Division
Huntsville, Alabama

http://www.collectspace.com/review/lcdrscott/SaturnIBV_IUS_DCD.pdf

Apollo 11 was landed on the moon using a computer that had 1,300 times less processing power than iPhone 5s



LVGC Hardware

- The LVGC was capable of executing **12,190 instructions per second**. For comparison, a **2012-era** microprocessor can execute 4 instructions per cycle at 3 GHz, achieving **12 billion instructions per second, one million times faster**.
- Its master clock ran at 2.048 MHz, but operations were performed bit-serially, with 4 cycles required to process each bit, 14 bits per phase, and 3 phases per instruction, for a basic time of **168 cycles = 82 μs** for a simple add. (A few instructions, such as multiply or divide, took a few times this value.)
- Memory was in the form of 13-bit syllables, each with a 14th parity bit.[1] Instructions were one syllable in size, while data words were two syllables (26 bits). **Main memory was random access magnetic core,** in the form of **4,096-word memory** modules. Up to 8 modules provided a maximum of **32,768 words of memory**. Ultrasonic delay lines provided temporary storage. **~ 106 KB**
- For reliability, the LVDC used **triple redundant logic** and a voting system. The computer included three identical logic systems. Each logic system was split into a seven-stage pipeline. At each stage in the pipeline, a voting system would take a majority vote on the results, with the most popular result being passed on to the next stage in all pipelines. This meant that, for each of the seven stages**, one module in any one of the three pipelines could fail, and the LVDC would still produce the correct results.** The result was an estimated reliability of **99.6% over 250 hours** of operation, which was far more than the few hours required for an Apollo mission.
- With four memory modules, giving a total capacity of **16,384 words**, the computer weighed **72.5 lb (32.9 kg),** was 29.5×12.5×10.5 inches in size (74×32×27 cm) and consumed **137 watts**. **53 KB**

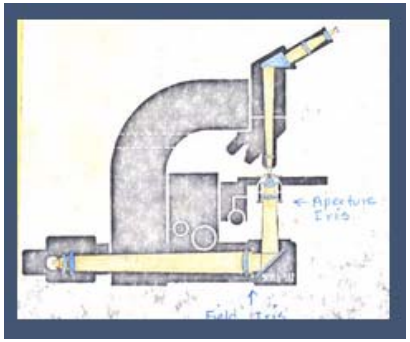
Construction

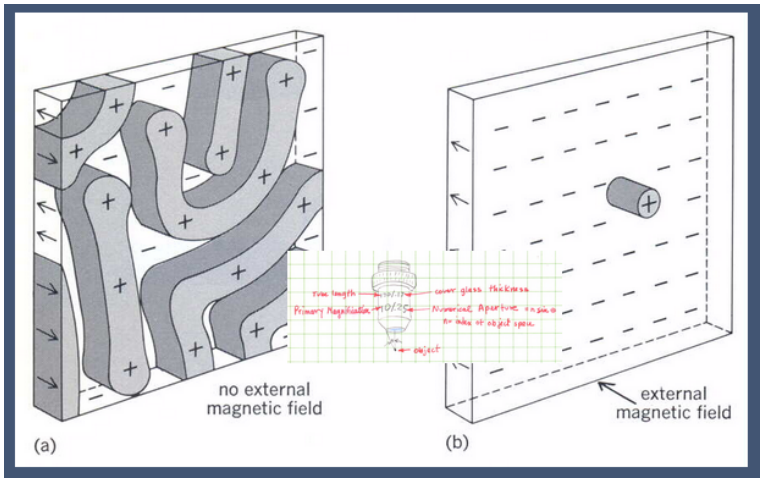
- The LVDC was approximately 30 inches wide, 12.5 inches high, and 10.5 inches deep and weighed 80 pounds. **The chassis was made of magnesium-lithium alloy** LA 141, chosen for its high stiffness, low weight, and good vibration damping characteristics. The chassis was divided into a 3 x 5 matrix of cells separated by walls through which **coolant was circulated to remove the 138 Watts** of power dissipated by the computer. Slots in the cell walls held "pages" of electronics. The decision to cool the LVDC by circulating coolant through the walls of the computer was unique at the time and allowed the LVDC and LVDA (part-cooled using this technique) to be placed in one cold plate location due to the three dimensional packaging. The cold plates used to cool most equipment in the Instrument Unit were inefficient from a space view although versatile for the variety of equipment used. The alloy LA 141 had been used by IBM on the Gemini keyboard, read out units, and computer in small quantities and the larger frame of the LVDC was produced from the largest billets of LA 141 cast at the time and subsequently CNC machined into the frame.

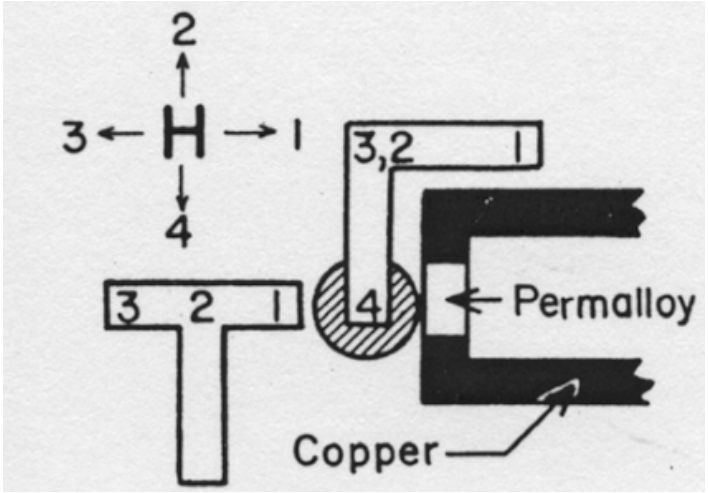
- A **page consisted of two 2.5 x 3-inch boards back to back and a magnesium-lithium frame to conduct heat to the chassis.** The **12-layer boards** contained signal, power, and ground layers and connections between layers were made by plated-through holes.

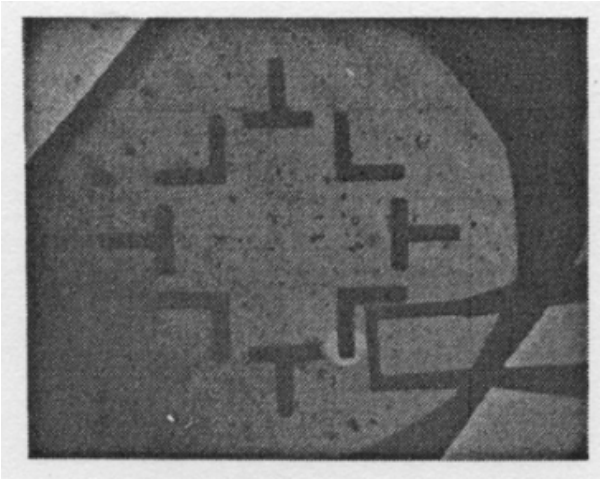
- Up to **35 alumina squares 0.3 x 0.3 x 0.070 inch** could be reflow soldered to a board. These alumina squares had conductors silk screened to the top side and resistors silk-screened to the bottom side. Semiconductor chips 0.025 x 0.025 inch, each containing either one transistor or two diodes, were reflow soldered to the top side. The complete module was called a unit logic device. The unit logic device (ULD) was a smaller version of IBM's Solid Logic Technology **(SLT) module, but with clip connections. Copper balls were used for contacts between the chips and the conductive patterns.**

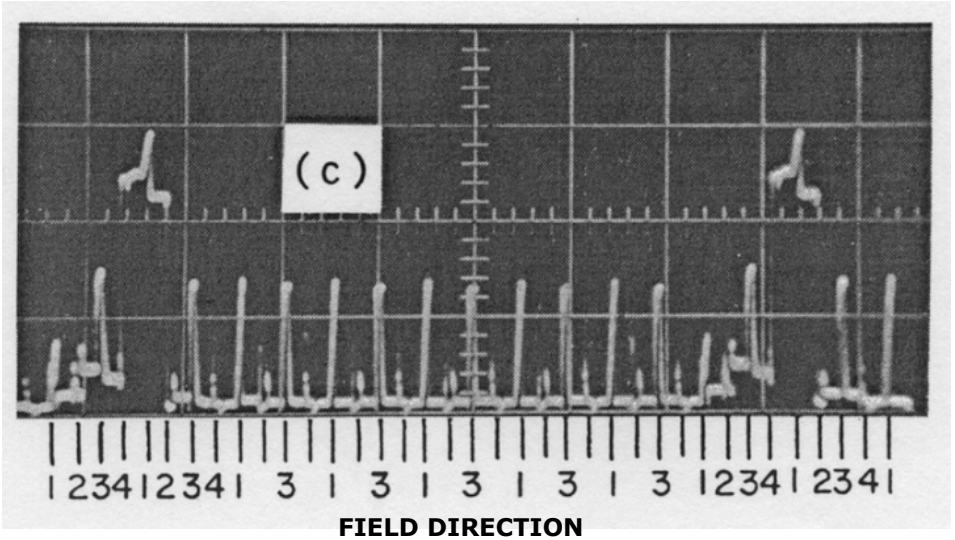
Bubble Memory



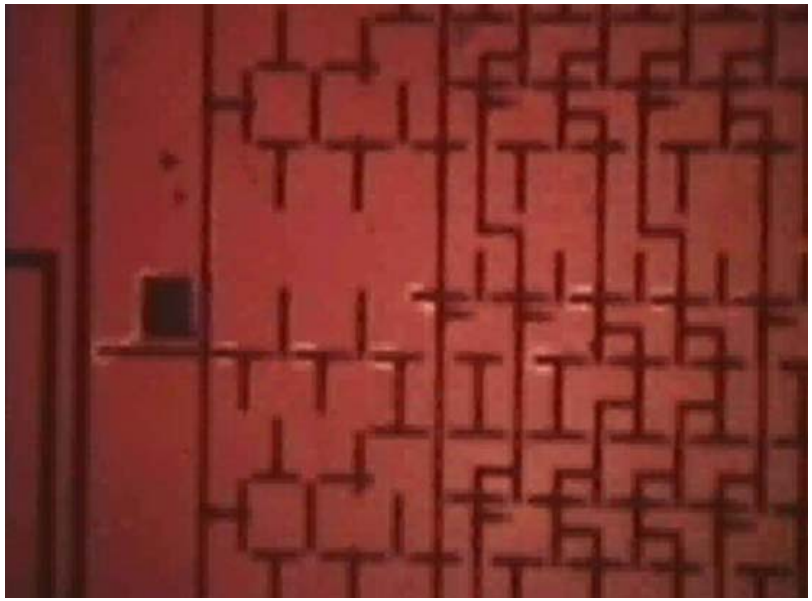




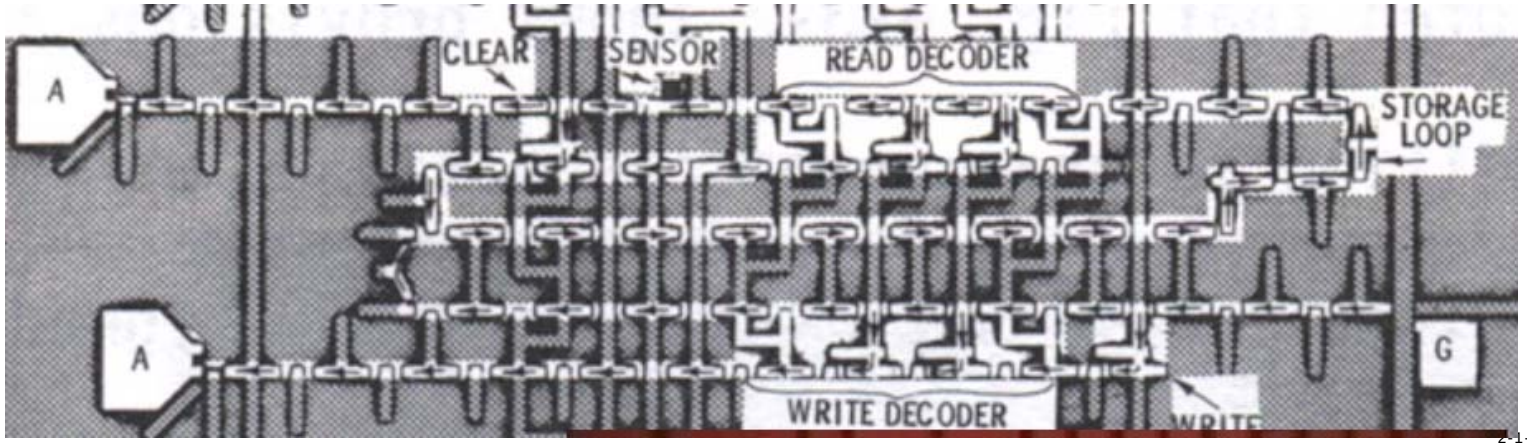




FIELD DIRECTION



Mag Bubble Video



Wireless Long Range Communication

- **NBS, 1954**
- **Device for digital communication by radio wave across the continent.**
- **Compress the data and bounce the beam off of a meteor trail.**

Listen

Tape to xmitter 36 ft / s
= 777 K bits / s

x 26,000

6 char / s * 5 bits / char = 30 bits/s
To Tape at 1 inch / min = 1800 bits / in.